Analysis of a New Peak and Hold Circuit for Electromagnetic Pulse

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Abstract— **This paper proposed new presented of the circuit design for the peak and hold circuit with feedback of sensing the electromagnetic pulse(EMP) accepting process signal transfer for producing a holding voltage levels corresponding to peak the amplitude and to raise the holding effect. The peak and hold circuit without feedback as a comparator to compare the reaction of the raising time from the process signal of EMP. Based on the feedback configuration and clamping network could add the charging current ratio for the storage capacitor to improve the whole reaction of the peak and hold detection for the raising time of the process signal.**

Keywords— **feedback, peak and hold, EMP, clamping network**

1. INTRODUCTION

Mostly the peak detectors response very fast to peak the amplitude and to detect high bandwidth signals, but usually has single one peak detector involved a diode and capacitor. This paper proposes design utilizing RC low pass filter to average the output signal [2] and control the detective duration time. For sensing EMP signal, the peak detector needs very fast to peak and considers increasing the holding effect to catch the signal, so adding the second peak detector to rise the efficiency. Here the combination of the two peak detectors is called the new peak and hold detector.

At a suitable distance from the EMP generator it can produce maximum voltage of 300kv, uses the solenoid let it be horizontal as the sensor to receive the EMP and transfer the process signal to holding voltage levels corresponding to peak the amplitude and to raise the holding effect by the peak and hold circuit measured from a wide-band oscilloscope. In this paper, we design the peak and hold circuit with feedback compare to without feedback circuit to discuss the feedback configuration for the reaction of the raising time.

2. CIRCUIT DESCRIPTION

Generally measuring the peak of a signal includes the use of a diode. However, the input signal has to be larger to overcome the turn-on voltage to detect. Therefore, the input signal has a mediocre error on the common circuit of a simple diode peak detector [1, 2]. For the proposed design of the two new peak and hold circuits involved simple diode peak detectors for detecting EMP signal to probe into the reaction of the raising time.

The peak and hold circuit without feedback composed of the two simple diode peak detectors is shown in Fig. 1 that couldn't use NPN transistors because the input signal would reduce from the base-emitter voltages and diodes turn-on voltages if the input signal hasn't to be larger that would cause the first stage to peak the signal drop down and lead to the second stage which acceptable signal is too low to detect. In order to improve the above problems adopted Q1, Q2, PNP transistors to enhance the signal process avoid base-emitter decreasing.

The circuits C1, R4, C2, R6, provide the low-pass filtering to average the peak and hold signal [2]. Based on this design as the comparator make up of two simple diode peak detectors compare with feedback system to observe different reaction of the raising time.

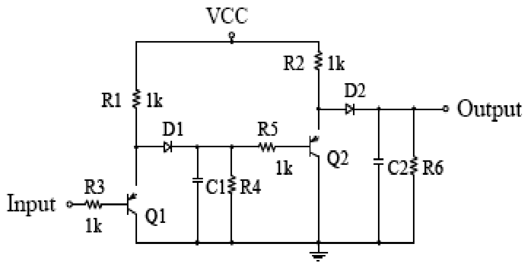

Fig.1 The peak and hold circuit without feedback

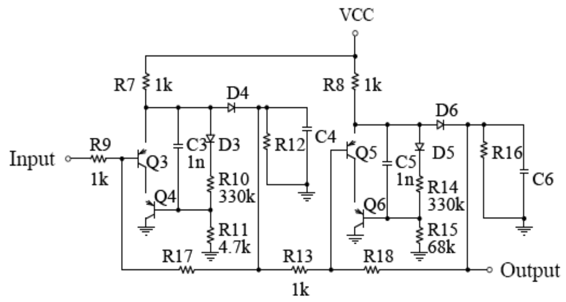

Fig.2 The peak and hold circuit with feedback

A schematic drawing of the peak and hold circuit with feedback is shown in Fig. 2 and using feedback configuration the circuit can provide better accuracy and sensitivity to compensate the diode turn-on voltage and rise up the reaction time. The input stage used high performance PNP transistors Q3, Q5 whose output are fed into both diodes D4, D6 which circuits be alike simple diode peak detectors. The diodes D4, D6 are connected to the storage capacitors C4, C6 which are fed back to the input through R17, R18. These resistances control the gain of the circuit that can adjust input signals to prevent the signal too low to reduce the whole peak and hold signals efficiency [1, 2, 3].

The diodes D3, D5 of the clamping network are always held on by the current source, for input signal greater than the signal at the output of peak and hold circuit then D4, D6 forward biased, the output signals rise up through the feedback configuration to match the input signals, as the input signals less than the peak and hold at the output signals lead to D4, D6 off.

The second feedback loop is formed when the bases of Q4, Q6, PNP transistors are pull down by the output signals of the front Q3, Q5 through the D3, D5 of forward bias then form feedback loop. The resistances of R10, R14 can ensure to establish Q4, Q6 active and to rise up producing the charge-discharge current [1].

The clamping network function can increase the charging current and output signals to prevent the front Q3, Q5 feedback into open loop behavior and to compensate for the diode turn-on voltage [1, 2].

3. COMPUTER SIMULATION

Computer simulation of transient behavior uses pulse source instead of the active EMP, to analyze the circuit design of the feedback configuration. To prove that can improve the circuit without feedback rising up the efficiency have faster reaction time to detect the signal.

The two circuits design let all stages have the simple diode peak detectors and that are at the same conditions, the first stage R4=R12=47kΩ, C1=C4=0.1μF, the second stage R6=R16=1MΩ, C2=C6=27nF, As the results are shown in Fig. 3 and Fig. 4, the solid line is the input signal.

According to simulation results compare with the first stage, the feedback circuit is 149.1(μs) and without-feedback is 187.29(μs), the former can improve the reaction of the raising time is 20.39%. The second stage of the feedback circuit is 152.81(μs) and without-feedback is 212.83(μs) that the feedback circuit to rise up 28.2%, thus it can be seen, the circuit without-feedback in order to increase holding effect of the second stage to catch the signal, but the circuit involved two simple diode peak detectors exist the mediocre error 10% [1, 2], then the second stage has the more signal error lead to reaction of raising time weaken.

From the simulated results, based on the feedback configuration used R17 and R18 to control the gain, feedback to adjust matching the input signal. Clamping network increases the charging current to compensate the mediocre error, the first stage rises up the raising time is 20.39% and the second stage improves the reaction time effect better than the without feedback circuit is 28.2%.

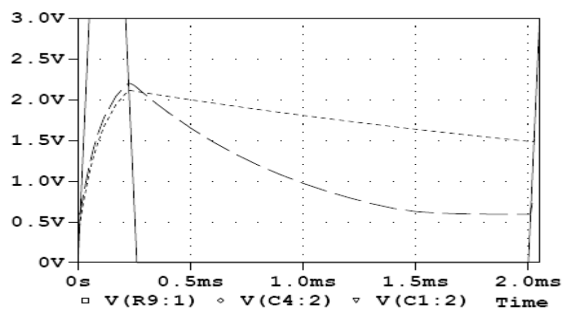

Fig.3 Comparison the circuit of simulations with feedback (long dotted line) and without-feedback (short dotted line) at the first stage

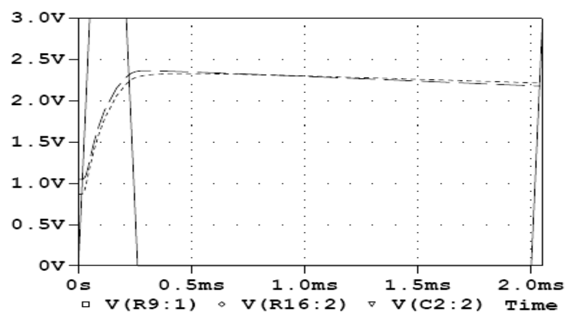

Fig.4 Comparison the circuit of simulations with feedback (long dotted line) and without-feedback (short dotted line) at the second stage

The peak and hold circuit with feedback although retains the simple diode peak detectors, but in clamping network can compensate the diode turn-on voltage and to form a feedback loop. The feedback loop can keep the input signal from dropping, beyond the function compare to without feedback circuit and it can improve the raising time completely fast to peak the amplitude and keep the holding reaction to improve the whole efficiency.

4. EXPERIMENT RESULT

After the design and simulation of circuit, the peak and hold circuit is made for EMP measuring at a suitable distance to detect. We have built a EMP generator with a solidstate relay (SSR) to control the trigger time and a NI-DAQ USB between EMP and computer. The Measurement structure is shown in Fig. 4, utilizing solenoid as the sensor being horizontal to receive the EMP through the process signal producing the holding voltage levels to peak and hold detective the amplitude.

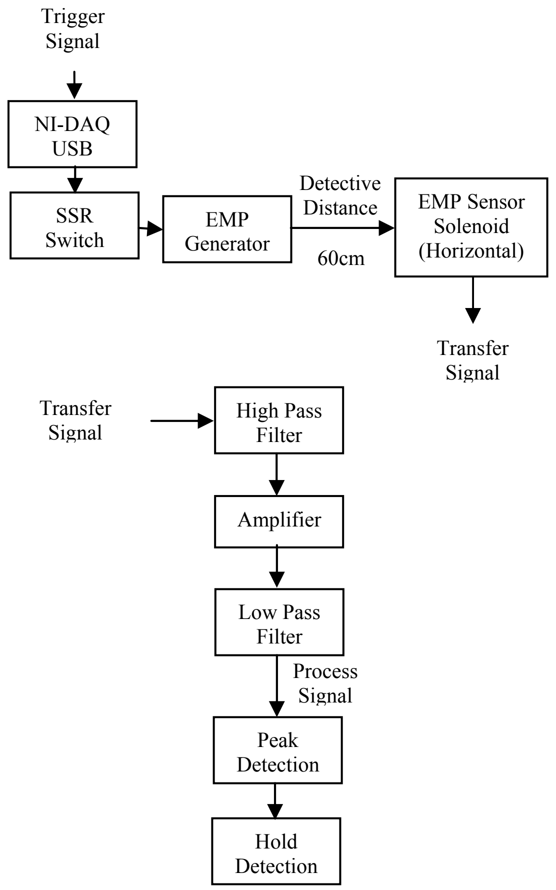

Fig.4 Measurement and circuit structure for EMP

The measurement results from oscilloscope to get the data transfer to diagrams are shown in Fig.5 to Fig.8, the tables are EMP signals sampling data comparison with the two design peak and hold circuits of stages, respectively.

From the tables, one can see the first stage in feedback system which can improve the reaction of the raising time about 21.3% and second stage 40.6%. Between the measurement and the simulated results, according the measurement data we can know the circuit with feedback system results that conformed to the computer simulation and improved the efficiency of reaction time fast to peak and hold detection.

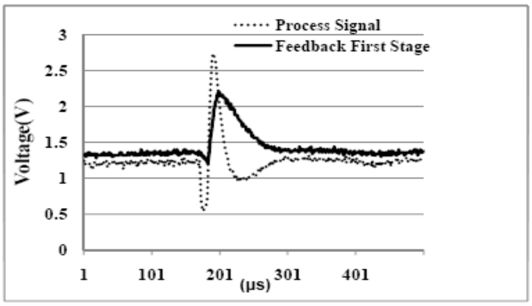

Fig. 5 The first stage of sensing circuit with feedback loop under the EMP test experiment

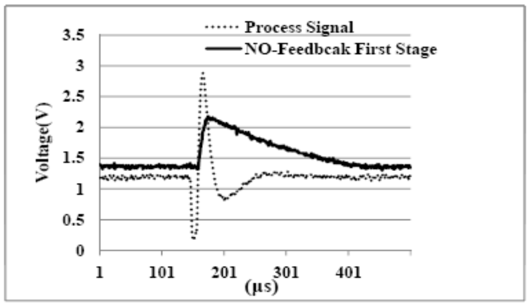

Fig. 6 The first stage of sensing circuit without feedback loop under the EMP test experiment

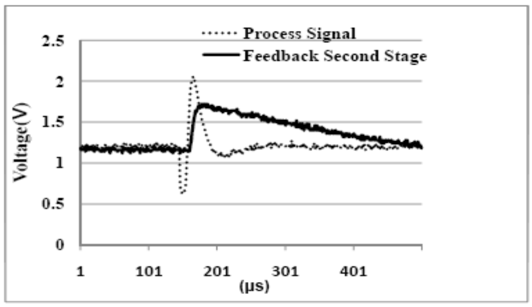

Fig. 7 The second stage of sensing circuit with feedback loop for the same condition of EMP testing

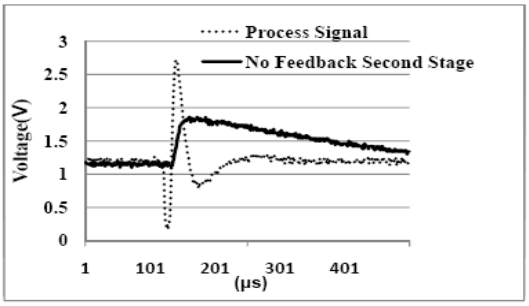

Fig. 8 The second stage of sensing circuit without feedback loop for the same condition of EMP testing

TABLE 1

COMPARISON TABLE OF THE FIRST STAGE

	Process Signal	First Stage No Feedback	Process Signal	First Stage Feedback
Raised Time	50.18µs	84.13µs	51.66µs	64.16µs
	50.31µs	83.33µs	51.01µs	74.00µs
	48.36µs	86.07µs	50.30µs	57.70µs
	50.73µs	88.00µs	49.85µs	77.50µs
	50.00µs	84.26µs	48.45µs	62.00µs

TABLE 2

COMPARISON TABLE OF THE SECOND STAGE

	Process Signal	Second Stage No Feedback	Process Signal	Second Stage Feedback
Raised Time	62.19µs	103.00µs	63.66µs	52.10µs
	65.74µs	135.00µs	68.33µs	79.46µs
	62.51µs	116.80µs	69.77µs	72.08µs
	62.56µs	101.70µs	63.33µs	67.33µs
	62.36µs	103.00µs	66.83µs	61.33µs

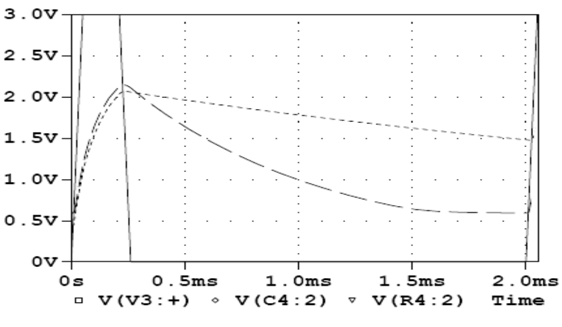

Fig. 9 Comparison the circuit of parasitic effect simulations with feedback (long dotted line) and without-feedback (short dotted line) at the first stage

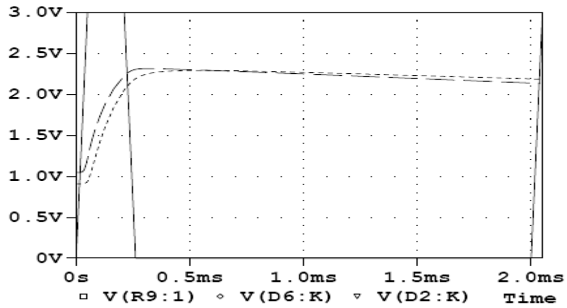

Fig. 10 Comparison the circuit of parasitic effect simulations with feedback (long dotted line) and without-feedback (short dotted line) at the second stage

Based on computer simulation, we also want to invesitgate the parasitic effect and measurement environment which affect difference between the experiments and simulations. Therefore, adding the parasitic capacitance in all biopolar of simulation, the simulations are also at the same input signal as Fig. 9 and Fig. 10.

The first stage comparison of feedback circuit is 146.9(µs) and without-feedback is 189.58(µs). That feedback system of first stage rises up the reaction is 22.5%. The second stage comparison of feedback circuit is 153.78(µs) and without-feedback is 249.62(µs). That feedback system of second stage rises up the reaction is 38.4%. From the results of theoretical design being to tally with measurement proportion of the comparison with a new peak and hold circuit with feedback.

5. CONCLUSIONS

A new peak and hold circuit is proposed with two peak detectors and a feedback loop is added to enhance the signal pickup for EMP measurement. The peak and hold circuit without feedback contributed by simple diode peak detectors conventionally uses PNP transistors to increase the input singal better than NPN transistors. We have designed the peak and hold circuit with feedback system although that inolved simple diode peak detectors, but utilizign the clamping network to compensate the diode turn-on voltage and feedback system to adjust input signals.

We have built a EMP testing equipment to measure the response time and transient behavior of the proposed circuit and the conventional circuit. The first stage in feedback system can improve 21.3% to peak the amplitude, and second stage rise up 40.6% to hold, that increased the whole efficiency being supior to the peak and hold circuit without feedback. The peak and hold circuit with feedback can detect the EMP signal with high efficiency, and make a great difference from the circuit wihout-feedback with raising time being weaken owing to the diode turn–on voltage accumulated force to the signal which reduce the second stage holding efficiency.

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